

What is claimed is:

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- 1 A method configuring packets, said packets each having a training portion and a data portion to set a receiver, comprising the step of:

forming said training portion by serially connecting K sequences (where K is an integer of 2 or more), each of said K sequences being formed of N symbols (where N is an integer of 2 or more).

- 10 2 The packet configuring method defined in Claim 1, wherein said the auto-correlation function of said N symbol sequence is in an impulse state.

- 15 3 A packet receiver that receives packets each which is formed of a training portion and a data portion to initialize of said receiver, said training portion being formed by serially connecting K sequences (where K is an integer of 2 or more), each of said K sequences being formed of N symbols (where N is an integer of 2 or more), comprising:

20 frequency-offset estimation means for estimating a frequency offset based on a phase difference between two neighboring sequences of K sequences a received packet, each of said K sequences being formed of N symbols; frequency-offset compensation means for

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compensating a frequency offset contained in
said received packet based on said frequency
offset estimation value; and

channel impulse response estimation means for
estimating an impulse response of a channel
based on an output of which the frequency
offset is compensated.

4 The packet receiver defined in Claim 3, wherein the
auto-correlation function of said N symbol sequences
is in an impulse state; and wherein said channel
impulse response estimation means comprises means
for estimating a channel impulse response based on a
sequence of which the auto-correlation function is
in an impulse state and a received training sequence.

5 The packet receiver defined in Claim 3, wherein said
frequency offset estimation means comprises:

a delay circuit for delaying said received
packet by a transmission period of time of a
sequence of N-symbol sequences;

a phase difference detection circuit for
detecting a phase difference between an
output of said delay circuit and said
received packet;

an integrator for integrating a detection output
of said phase difference detection circuit

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a divider circuit for dividing an output of said integrator by a product of N and M.

~~6~~ The packet receiver defined in Claim ~~3~~², wherein said impulse response estimation means outputs a channel impulse response estimation value after inputting a pulse representing that said frequency offset estimation means has completed frequency offset estimation.

7 A packet receiver for receiving packets, each of said packets having a training portion and a data portion to initially set a receiver, said training portion being formed by serially connecting K sequences (where K is an integer of 2 or more), each of K sequences being formed of N symbols (where N is an integer of 2 or more), comprising:

frequency offset estimation means for detecting a phase difference between a sequence received prior to NT (where T is a continuous time of one symbol) and a currently received sequence and then estimating a frequency offset based on said phase difference;

frequency offset compensation means for

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compensating said frequency offset by
rotating the phase of a received signal in
the frequency offset compensation direction
based on a frequency offset estimation value;
and

channel impulse estimation means for estimating
an impulse response of a channel based on an
output from an output of which the frequency
offset is compensated.

8 The packet receiver defined in Claim 7, wherein the
auto-correlation function of said N symbol sequences
is in an impulse state; and wherein said channel
impulse response estimation means comprises means for
estimating a channel impulse response based on a
sequence of which the auto-correlation function is in
an impulse state and a received training sequence.

8 9 The packet receiver defined in Claim 7, wherein said
impulse response estimation means outputs a channel
impulse response estimation value after inputting a
pulse representing that said frequency offset
estimation means has completed frequency offset
estimation.

10 A packet receiving method for receiving packets,
each of said packets having a training portion and
a data portion to initially set a receiver, said

training portion being formed by serially
connecting K sequences (where K is an integer of 2
or more), each of said K sequences being formed of
N symbols (where N is an integer of 2 or more),
comprising the steps of:

estimating a frequency offset based on a phase
difference between two neighboring sequences
of K sequences of a received packet, each of
K sequences being formed of N symbols;

compensating a frequency offset contained in
said received packet based on a frequency
offset estimation value; and

estimating an impulse response of a channel
based on a received packet of which the
frequency offset is compensated.

11 The packet receiving method defined in Claim 10,
wherein said step of estimating an impulse response
of said channel comprises estimating a channel
impulse response by making the auto-correlation
function of said N symbol sequence in an impulse
state and detecting a peak value of an auto-
correlation value between a received signal and an
N symbol sequence.

12 The packet receiving method defined in Claim 10,
wherein said step of estimating an impulse response

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of said channel comprises the step of outputting a channel impulse response estimation value after frequency offset estimation has been completed.